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PCI-SIG ENGINEERING CHANGE REQUEST

1. PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	Voltage Indication for PCIe BGA SSD 16x20
DATE:	October 31, 2018
AFFECTED DOCUMENT:	PCIe M.2 Specification_Rev1.1
SPONSOR:	Intel, Dell, Toshiba Memory Corp, WDC

Part I

1.1. Summary of the Functional Changes

This proposal repurposes five RFU pins in the 16 mm x 20 mm BGA ball map to be optionally used for indicating PWR1, PWR2, and PWR3 supply voltage requirements to the Platform.

1.2. Benefits as a Result of the Changes

The Platform and the BGA module may benefit from hardware-indicated voltage supply requirements in-system, simplifying BOM variations per platform and associated costs.

1.3. Assessment of the Impact

This change updates the pin assignments for 16 x 20 BGA. It has no impact on the physical 16 mm x 20 mm form factor or any of the other BGA form factors. The change does require updates to signal definitions and parameters throughout Section 3.4: “BGA SSD Interface Signals”, relevant to the new voltage ID pin definition. 16 x 20 pinouts in Section 3.4 and Section 5 require updates as well.

1.4. Analysis of the Hardware Implications

This document defines the optional usage of five pins for 16 x 20 BGA that previously had reserved functionality. Used together, 32 unique output voltage combinations across the PWR_1, PWR_2, and PWR_3 supplies are possible. There is no change to voltage sequencing or other electrical requirements. There is no requirement for BGA modules that utilize the optional 5 voltage ID pins to be backwards compatible with existing Platforms that do not support the new pin definition. The Platform design is responsible for ensuring BGA module compatibility.

1.5. Analysis of the Software Implications

N/A.

1.6. Analysis of the C&I Test Implications

N/A.

[Editor's note: Existing M.2 v1.1 text is black. New text is marked in blue with underscore. Material to be deleted ~~is red with strikethrough~~.]

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3.4 BGA SSD Interface Signals

Table 39. BGA SSD System Interface Signal Table

< Editor's Note: At end of section in table>

Interface	Signal Name	I/O	Function	Voltage
SSD Specific Optional Signals	PWR_ID[0:4]	O	Voltage requirement indication to Platform. The Platform uses the combination of these 5 signals to determine the BGA module voltage requirements for each of the PWR_1, PWR_2, and PWR_3 power supplies.	0 V/NC

< Editor's Note: After 3.4.5.7>

3.4.5.new. **PWR_ID[0:4]**

The PWR_ID[0:4] signals are optional signals. When supported by the BGA module, the combination of the 5 signals together are used to inform the Platform which voltage level is required on each of the PWR_1, PWR_2, and PWR_3 power supplies.

Note: Platforms that support BGA voltage indication must support a mechanism for sensing the state of all PWR_ID[0:4] pins before or in conjunction with enabling the voltage rail that supplies each of the PWR_1, PWR_2, and PWR_3 power supply domains to ensure the BGA module is not damaged (e.g., direct Platform voltage regulation subsystem connection to influence output levels, pin state decoding using pull-ups and logic located on the Platform, or alternative Platform implementation approach).

Table xx. PWR_ID[0:4] signal definitions

PWR_ID[4:0] Voltage Indication Signal Configuration					PWR_1, PWR_2, PWR_3 Voltage		
PWR_ID0 (pin D15)	PWR_ID1 (pin F15)	PWR_ID2 (pin H14)	PWR_ID3 (pin C14)	PWR_ID4 (pin C13)	PWR_1	PWR_2	PWR_3
NC	NC	NC	NC	NC	RFU	RFU	RFU
GND	NC	NC	NC	NC	2.5 V	1.2 V	0.9 V
NC	GND	NC	NC	NC	2.5 V	1.2 V	1.1 V

PWR_ID[4:0] Voltage Indication Signal Configuration					PWR_1, PWR_2, PWR_3 Voltage		
PWR_ID0 (pin D15)	PWR_ID1 (pin F15)	PWR_ID2 (pin H14)	PWR_ID3 (pin C14)	PWR_ID4 (pin C13)	PWR_1	PWR_2	PWR_3
GND	GND	NC	NC	NC	2.5 V	1.2 V	RFU
NC	NC	GND	NC	NC	2.5 V	1.2 V	1.2 V
GND	NC	GND	NC	NC	RFU	RFU	RFU
NC	GND	GND	NC	NC	RFU	RFU	RFU
GND	GND	GND	NC	NC	RFU	RFU	RFU
NC	NC	NC	GND	NC	RFU	RFU	RFU
GND	NC	NC	GND	NC	2.5 V	1.8 V	0.9 V
NC	GND	NC	GND	NC	2.5 V	1.8 V	1.1 V
GND	GND	NC	GND	NC	2.5 V	1.8 V	RFU
NC	NC	GND	GND	NC	2.5 V	1.8 V	1.2 V
GND	NC	GND	GND	NC	RFU	RFU	RFU
NC	GND	GND	GND	NC	RFU	RFU	RFU
GND	GND	GND	GND	NC	RFU	RFU	RFU
NC	NC	NC	NC	GND	RFU	RFU	RFU
GND	NC	NC	NC	GND	3.3 V	1.2 V	0.9 V
NC	GND	NC	NC	GND	3.3 V	1.2 V	1.1 V
GND	GND	NC	NC	GND	3.3 V	1.2 V	RFU
NC	NC	GND	NC	GND	3.3 V	1.2 V	1.2 V
GND	NC	GND	NC	GND	RFU	RFU	RFU
NC	GND	GND	NC	GND	RFU	RFU	RFU
GND	GND	GND	NC	GND	RFU	RFU	RFU
NC	NC	NC	GND	GND	RFU	RFU	RFU
GND	NC	NC	GND	GND	3.3 V	1.8 V	0.9 V
NC	GND	NC	GND	GND	3.3 V	1.8 V	1.1 V
GND	GND	NC	GND	GND	3.3 V	1.8 V	RFU
NC	NC	GND	GND	GND	3.3 V	1.8 V	1.2 V
GND	NC	GND	GND	GND	RFU	RFU	RFU
NC	GND	GND	GND	GND	RFU	RFU	RFU
GND	GND	GND	GND	GND	RFU	RFU	RFU

3.4.6. BGA SSD Soldered-Down Module Pin-out

All pinout tables in this section are written from the module point of view when referencing signal directions.

<Editor's Note: In Figure 104 replace text in cells:

D15: PWR_ID0~~RFU~~

F15: PWR_ID1~~RFU~~

H14: PWR_ID2~~RFU~~>

C14: PWR_ID3~~RFU~~

C13: PWR_ID4~~RFU~~

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	3.3 V	3.3 V	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	3.3 V	3.3 V	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PERp0	SATA-A- /PERn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNU	DNU	DNU
H				SATA-B+ /PETp0	SATA-B- /PETn0		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		RFU	RFU			
J	GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNU	DNU	DNU
K				PERp1	PERn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PETp1	PETn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS
P				PERp2	PERn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNU	JTAG_TDI	JTAG_TDO
T				PETp2	PETn2		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		RFU	RFU			
U	GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNU	SMB_CLK	SMB_DATA
V				PERp3	PERn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED1#/ DAS	RFU	3.3 V	3.3 V	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PETp3	PETn3	GND	DNU	DNU	3.3 V	3.3 V	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

= No Solder Ball

Figure 104. Type 1620 BGA Module-side Ballmap (Top View)

<Editor's Note: In Figure 105 replace text in cells:

D15: PWR_ID0~~RFU~~

F15: PWR_ID1~~RFU~~

H14: PWR_ID2~~RFU~~>

C14: PWR_ID3~~RFU~~

C13: PWR_ID4~~RFU~~

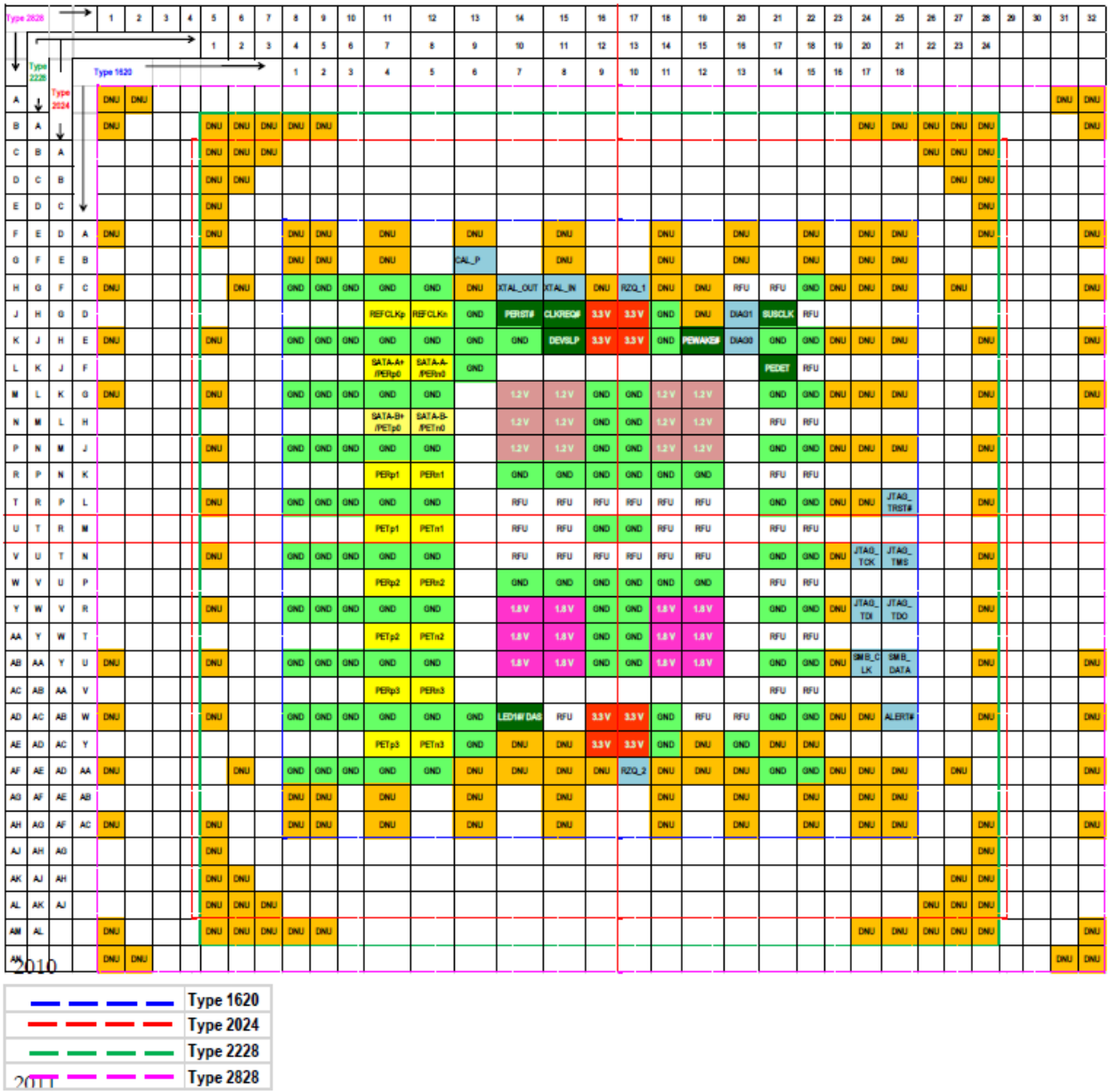

Figure 105. Type 1620 BGA Module-side Ballmap Surrounded by Type 2024, Type 2228, and Type 2828 Module-side Ballmaps (Top View)

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5. Platform Socket Pinout and Key Definitions

All pinouts tables in this section are written from the platform/system point of view when referencing signal directions.

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5.4. Soldered Down Pinouts Definitions

<Editor's Note: In Figure 111 replace text in cells:

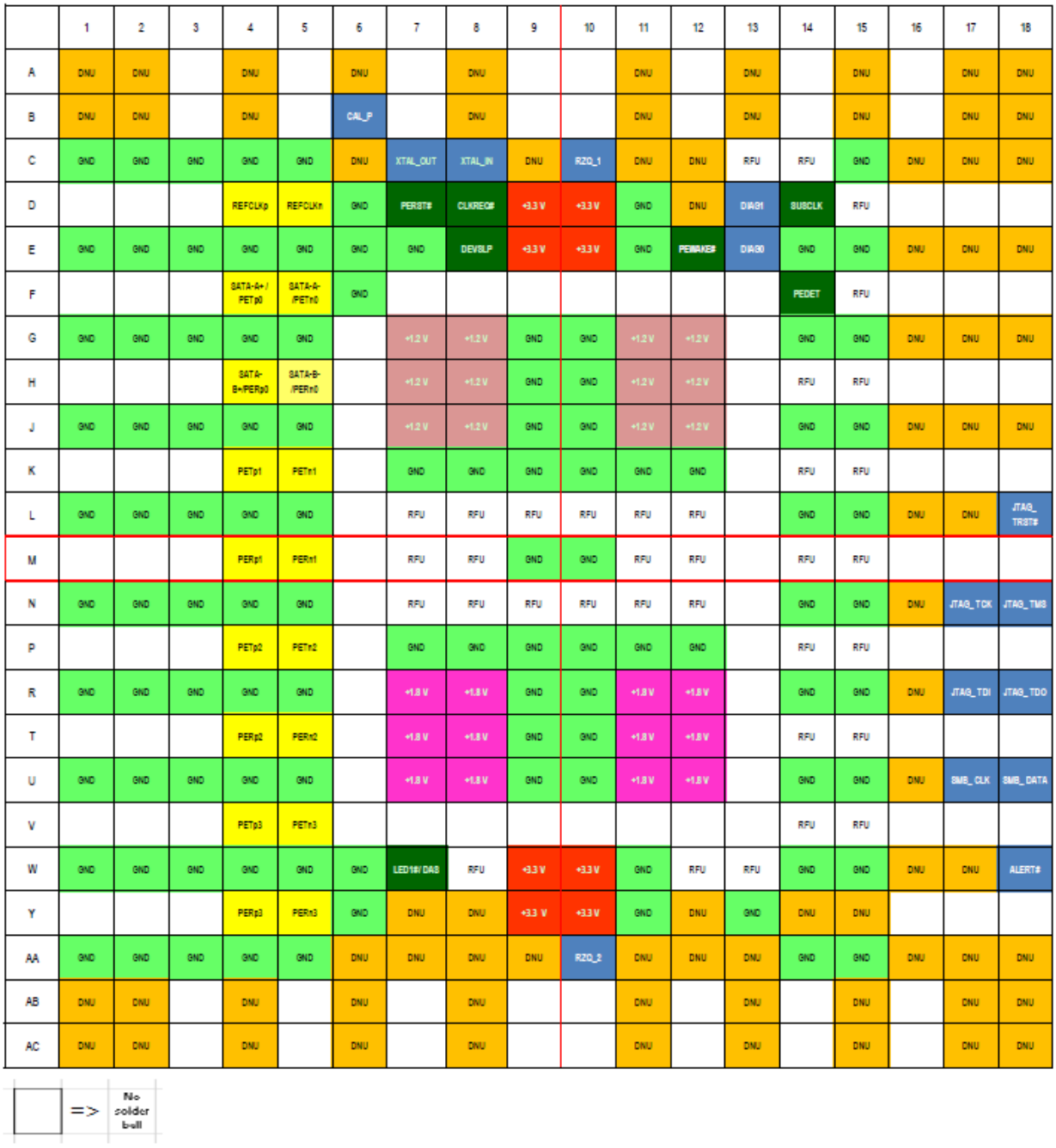
D15: PWR_ID0~~RFU~~

F15: PWR_ID1~~RFU~~

H14: PWR_ID2~~RFU~~>

C14: PWR_ID3~~RFU~~

C13: PWR_ID4~~RFU~~



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	+3.3 V	+3.3 V	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	+3.3 V	+3.3 V	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PETp0	SATA-A- /PETn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNU	DNU	DNU
H				SATA-B+/PERp0	SATA-B- /PERn0		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		RFU	RFU			
J	GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNU	DNU	DNU
K				PETp1	PETn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PERp1	PERn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS
P				PETp2	PETn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNU	JTAG_TDI	JTAG_TDO
T				PERp2	PERn2		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		RFU	RFU			
U	GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNU	SMB_CLK	SMB_DATA
V				PETp3	PETn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED1#/ DAS	RFU	+3.3 V	+3.3 V	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PERp3	PERn3	GND	DNU	DNU	+3.3 V	+3.3 V	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

=> No solder ball

Figure 111. Type 1620 BGA Pinout On Platform (Top View)

<Editor's Note: In Figure 112 replace text in cells:

D15: PWR_ID0~~RFU~~

F15: PWR_ID1~~RFU~~

H14: PWR_ID2~~RFU~~>

C14: PWR_ID3~~RFU~~

C13: PWR_ID4~~RFU~~

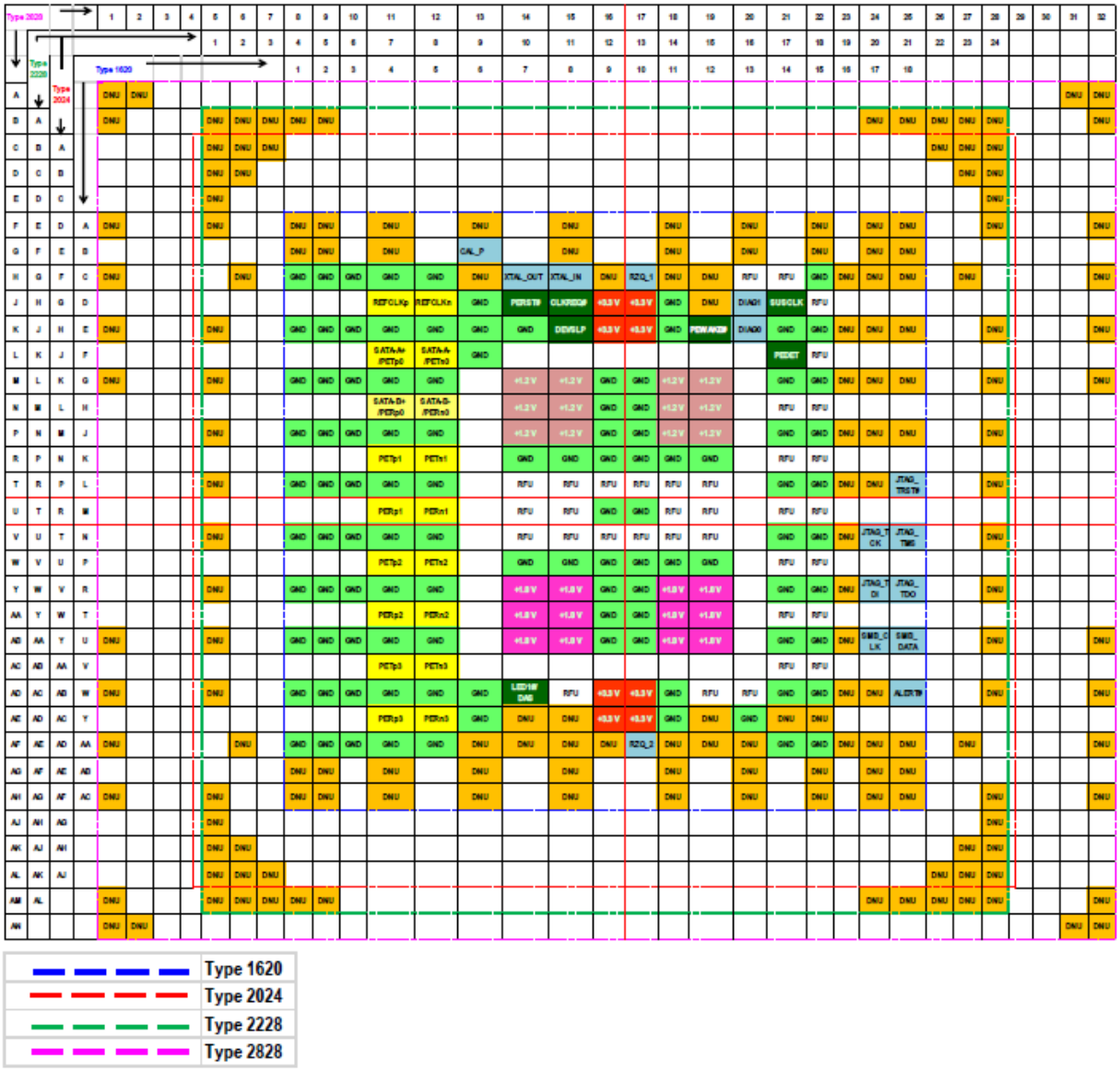


Figure 112. Type 1620, Type 2024, Type 2228, Type 2828 BGA Pinout On Platform (Top View)